

**REMARKS**

Claims 1 through 3 are currently pending in the application.

This amendment is in response to the Office Action of January 10, 2008.

**35 U.S.C. § 112 Claim Rejections**

Claims 2 and 3 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicant has amended the claimed invention for the presently claimed invention to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claims 2 and 3 are allowable under the provisions of 35 U.S.C. § 112.

**35 U.S.C. § 103(a) Obviousness Rejections**

Obviousness Rejection Based on Shils et al. (U.S. Patent 4,510,673) in view of Moosa et al. (U.S. Patent 5,822,218) and Jernigan (U.S. Patent 5,642,307)

Claims 1 through 3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shils et al. (U.S. Patent No. 4,510,673) in view of Moosa et al. (U.S. Patent No. 5,822,218) and Jernigan (U.S. Patent No. 5,642,307).

Applicant further submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

To establish a *prima facie* case of obviousness the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. *In re Royka*, 490 F.2d 981, 985 (CCPA 1974); *see also* MPEP § 2143.03. Additionally, the Examiner must determine whether there is “an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR Int’l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1740-1741, 167 L.Ed.2d 705, 75 USLW 4289, 82 U.S.P.Q.2d 1385 (2007). Further, rejections on obviousness grounds “cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *Id* at 1741, quoting *In re Kahn*, 441, F.3d 977, 988 (Fed. Cir. 2006). Finally, to establish a *prima facie* case of obviousness there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). Furthermore, the reason that would have prompted the combination and the reasonable expectation of success must be found in the prior art, common knowledge, or the nature of the problem itself, and not based on the Applicant’s disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006); MPEP § 2144. Underlying the obvious determination is the fact that statutorily prohibited hindsight cannot be used. *KSR*, 127 S.Ct. at 1742; *DyStar*, 464 F.3d at 1367.

Applicant asserts that any combination of the Shils et al. reference in view of Moosa et al. reference and the Jernigan reference does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 2, and 3 because any combination of such prior art does not teach or suggest all the claim limitations.

Turning to the cited prior art, the Shils et al. reference teaches or suggests directed to a system for identifying each chip with an inscribed identification on the back thereof that is both human and machine readable. The inscribed identification provides data used for quality control.

The Moosa et al. reference teaches or suggests system, method and computer program products for predicting defect-related failures in integrated circuits produced by an integrated circuit fabrication process.

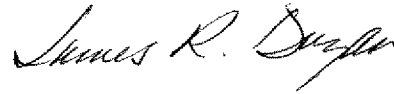
The Jernigan reference teaches or suggests an identification section fabricated onto a semiconductor integrated circuit which includes structure for storing die-specific information that characterizes a particular integrated circuit structure.

Applicant asserts any combination of the Shils et al. reference in view of Moosa et al. reference and the Jernigan reference does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 2, and 3 because any combination of such prior art does not teach or suggest the claim limitations calling for “establishing an enhanced reliability testing flag for an integrated circuit device resulting from fabrication errors and manufacturing deviations from a manufacturing process for an integrated circuit device of a plurality of integrated circuit devices”. Applicant asserts that the Shils et al. reference does not store any data on the chip regarding any requirement for further enhanced testing. The Moosa et al. reference does not predict any requirement for enhanced testing flag for any integrated circuit device resulting from fabrication errors and manufacturing deviations from a manufacturing process. The Moosa et al. reference merely uses a computer to predict problems based on circuit design from simulated reliability data, not from fabrication errors and manufacturing deviations from a manufacturing process for an integrated circuit device. The Jernigan reference merely teaches or suggests that an identification section is fabricated onto a semiconductor integrated circuit. Applicant asserts that any combination of the Shils et al. reference in view of Moosa et al. reference and the Jernigan reference merely teaches or suggests marking an identification section of a semiconductor chip to have possible simulated fabrication errors based on simulated reliability data for a particular integrated circuit design. Applicant asserts that such is not the claimed inventions of independent claims 1, 2, and 3. Therefore, claims 1, 2, and 3 are allowable.

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Applicant submits that claims 1, 2, and 3 are clearly allowable over the cited prior art.  
Applicant requests the allowance of claims 1, 2, and 3 and the case passed for issue.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "James R. Duzan". The signature is fluid and cursive, with the first name "James" being the most prominent.

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